

	<b>L #</b>	<b>Hit</b>	<b>S arch Text</b>	<b>DBs</b>
<b>1</b>	<b>L1</b>	<b>1241</b>	<b>257/723.ccls.</b>	<b>USP AT; US-P GPU B</b>
<b>2</b>	<b>L3</b>	<b>8</b>	<b>1 and (processor\$1 with communication)</b>	<b>USP AT; US-P GPU B</b>
<b>3</b>	<b>L2</b>	<b>5</b>	<b>1 and (micro\$1processor\$1 with communication)</b>	<b>USP AT; US-P GPU B</b>
<b>4</b>	<b>L4</b>	<b>7</b>	<b>3 not 2</b>	<b>USP AT; US-P GPU B</b>
<b>5</b>	<b>L5</b>	<b>862</b>	<b>257/777.ccls.</b>	<b>USP AT; US-P GPU B</b>
<b>6</b>	<b>L7</b>	<b>8</b>	<b>5 and (micro\$1processor\$1 with communication)</b>	<b>USP AT; US-P GPU B</b>
<b>7</b>	<b>L6</b>	<b>7</b>	<b>5 and (processor\$1 with communication)</b>	<b>USP AT; US-P GPU B</b>

	<b>L #</b>	<b>Hit</b>	<b>S arch T xt</b>	<b>DB</b>
<b>8</b>	<b>L8</b>	<b>444</b>	<b>257/728.ccls.</b>	<b>USP AT; US-P GPU B</b>
<b>9</b>	<b>L9</b>	<b>1</b>	<b>8 and (processor\$1 with communication)</b>	<b>USP AT; US-P GPU B</b>
<b>10</b>	<b>L10</b>	<b>1</b>	<b>8 and (micro\$1processor\$1 with communication)</b>	<b>USP AT; US-P GPU B</b>
<b>11</b>	<b>L11</b>	<b>2</b>	<b>9 10</b>	<b>USP AT; US-P GPU B</b>
<b>12</b>	<b>L12</b>	<b>5</b>	<b>1 and ((communication adj (device\$1 chip\$1)) and (micro\$1processor\$1 processor\$1))</b>	<b>USP AT; US-P GPU B</b>
<b>13</b>	<b>L13</b>	<b>8</b>	<b>1 and ((communication adj (device\$1 chip\$1 system\$1)) and (micro\$1processor\$1 processor\$1))</b>	<b>USP AT; US-P GPU B</b>
<b>14</b>	<b>L14</b>	<b>3</b>	<b>13 not 12</b>	<b>USP AT; US-P GPU B</b>

	<b>L #</b>	<b>Hit</b>	<b>S arch T xt</b>	<b>DB</b>
<b>15</b>	<b>L15</b>	<b>2</b>	<b>8 and ((communication adj (d vice\$1 chip\$1)) and (micro\$1processor\$1 processor\$1))</b>	<b>USP AT; US-P GPU B</b>
<b>16</b>	<b>L16</b>	<b>30</b>	<b>((die\$1 dice) with (micro\$1processor\$1 processor\$1) with (communication\$1 adj (device\$1 system\$1)))</b>	<b>USP AT; US-P GPU B</b>
<b>17</b>	<b>L17</b>	<b>127</b>	<b>5 and microprocessor\$1</b>	<b>USP AT; US-P GPU B</b>
<b>18</b>	<b>L18</b>	<b>32</b>	<b>17 and (spacer\$1 interposer\$1)</b>	<b>USP AT; US-P GPU B</b>
<b>19</b>	<b>L19</b>	<b>8</b>	<b>18 and (communication\$1 telecommunication\$1)</b>	<b>USP AT; US-P GPU B</b>
<b>20</b>	<b>L20</b>	<b>404</b>	<b>333/247.ccls.</b>	<b>USP AT; US-P GPU B</b>
<b>21</b>	<b>L21</b>	<b>24</b>	<b>20 and (micro\$1processor\$1 processor\$1)</b>	<b>USP AT; US-P GPU B</b>

	<b>L #</b>	<b>Hit</b>	<b>Sear h T xt</b>	<b>DB</b>
<b>22</b>	<b>L22</b>	<b>13</b>	<b>21 and (communication\$1 telecommunication\$1)</b>	<b>USP AT; US-P GPU B</b>
<b>23</b>	<b>L23</b>	<b>1857</b>	<b>343/702.ccls.</b>	<b>USP AT; US-P GPU B</b>
<b>24</b>	<b>L24</b>	<b>174</b>	<b>23 and (micro\$1processor\$1 processor\$1)</b>	<b>USP AT; US-P GPU B</b>
<b>25</b>	<b>L25</b>	<b>3</b>	<b>24 and (die dice)</b>	<b>USP AT; US-P GPU B</b>
<b>26</b>	<b>L27</b>	<b>0</b>	<b>26 and (bare adj chip\$1)</b>	<b>USP AT; US-P GPU B</b>
<b>27</b>	<b>L26</b>	<b>29</b>	<b>24 and chip\$1</b>	<b>USP AT; US-P GPU B</b>
<b>28</b>	<b>L42</b>	<b>371</b>	<b>vigushin.xa.</b>	<b>USP AT; US-P GPU B</b>

	<b>L #</b>	<b>Hit</b>	<b>Sear h T xt</b>	<b>DB</b>
<b>29</b>	<b>L43</b>	<b>94</b>	<b>42 and (communication\$ telecommunication\$1)</b>	<b>USP AT; US-P GPU B</b>
<b>30</b>	<b>L44</b>	<b>4637 39</b>	<b>43 (cpu\$1 micro\$1processor\$1 processor\$1)</b>	<b>USP AT; US-P GPU B</b>
<b>31</b>	<b>L45</b>	<b>40</b>	<b>43 and (cpu\$1 micro\$1processor\$1 processor\$1)</b>	<b>USP AT; US-P GPU B</b>
<b>32</b>	<b>L46</b>	<b>517</b>	<b>361/803.ccls.</b>	<b>USP AT; US-P GPU B</b>
<b>33</b>	<b>L48</b>	<b>112</b>	<b>46 and (micro\$1processor\$1 processor\$1)</b>	<b>USP AT; US-P GPU B</b>
<b>34</b>	<b>L47</b>	<b>128</b>	<b>46 and (cpu\$1 micro\$1processor\$1 processor\$1)</b>	<b>USP AT; US-P GPU B</b>

	<b>L #</b>	<b>Hit</b>	<b>S ar h T xt</b>	<b>DBs</b>
<b>1</b>	<b>L1</b>	<b>274</b>	<b>361/306.3.ccls.</b>	<b>USP AT; US-P GPU B</b>
<b>2</b>	<b>L2</b>	<b>102</b>	<b>1 and (pd palladium)</b>	<b>USP AT; US-P GPU B</b>
<b>3</b>	<b>L3</b>	<b>51</b>	<b>(anodiz\$5 with (palladium pd))</b>	<b>USP AT; US-P GPU B</b>
<b>4</b>	<b>L4</b>	<b>11</b>	<b>3 and (capacitor\$1 condenser\$1)</b>	<b>USP AT; US-P GPU B</b>

	<b>L #</b>	<b>Hits</b>	<b>S ar h T xt</b>	<b>DB</b>
<b>1</b>	<b>L1</b>	<b>1</b>	<b>5781255.pn.</b>	<b>USP AT; US-P GPU B</b>
<b>2</b>	<b>L2</b>	<b>0</b>	<b>1 and (platinum pt)</b>	<b>USP AT; US-P GPU B</b>
<b>3</b>	<b>L3</b>	<b>262</b>	<b>(anodiz\$5 with (platinum pt))</b>	<b>USP AT; US-P GPU B</b>
<b>4</b>	<b>L4</b>	<b>53</b>	<b>3 and (capacitor\$1 condenser\$1)</b>	<b>USP AT; US-P GPU B</b>